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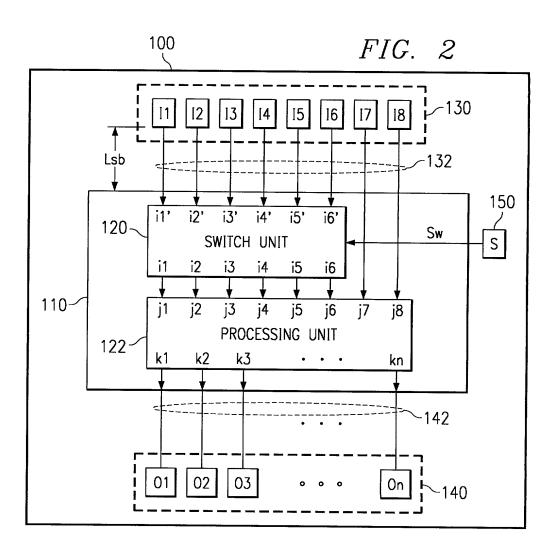


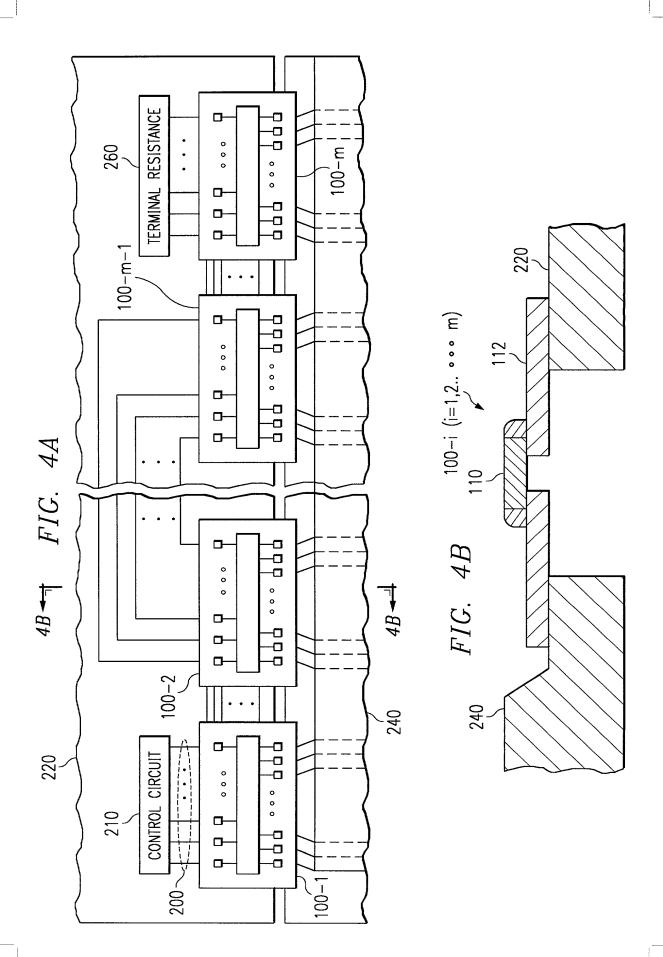
FIG. 3

Sw	INPUT	i1'	i2'	i3'	i4'	i5'	i6'
L	OUTPUT	i1	i2	i3	i4	i5	i6
Н		i6	i5	i4	i3	i2	i1

FIG. 9 D6-16 [6 16 D5-15 15 15 [4 D4 -**SOURCE** 14 **SOURCE** 14 **SOURCE** DEVICE DEVICE D3-13 13 DEVICE 13 D2-12 12 12

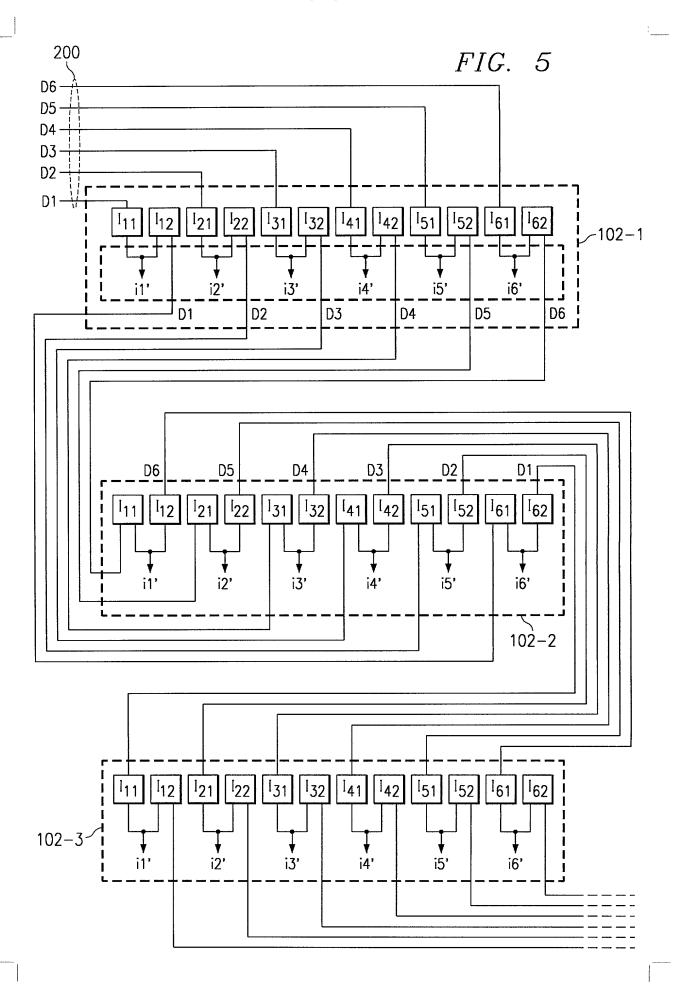
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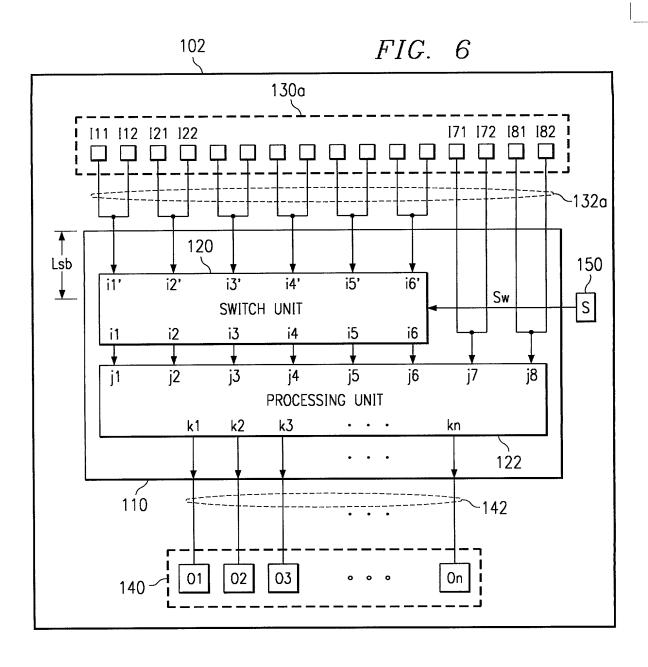
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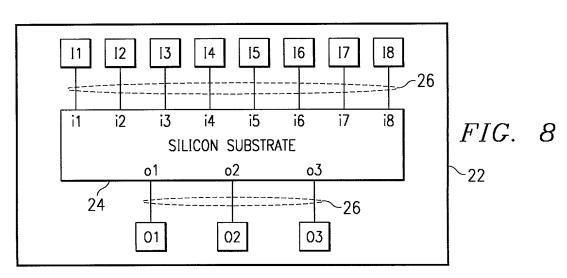


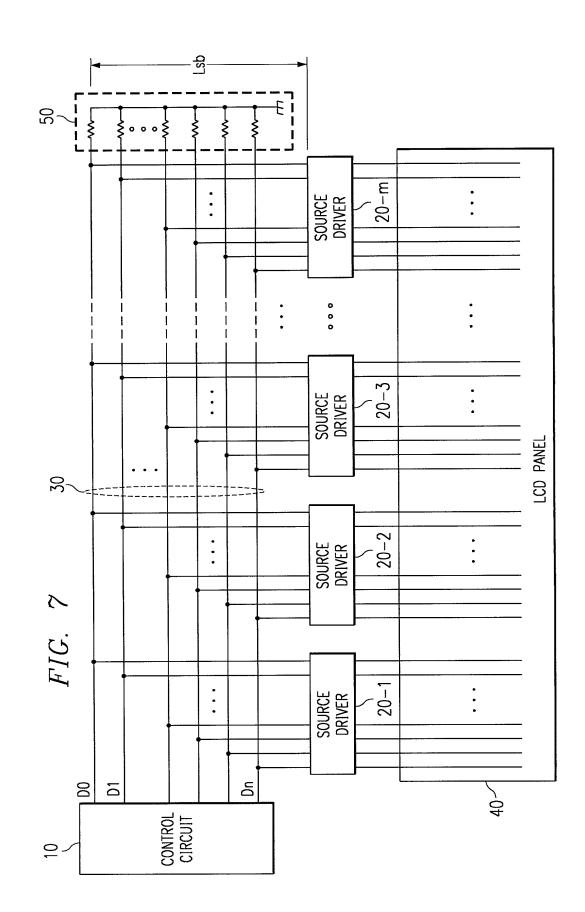
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